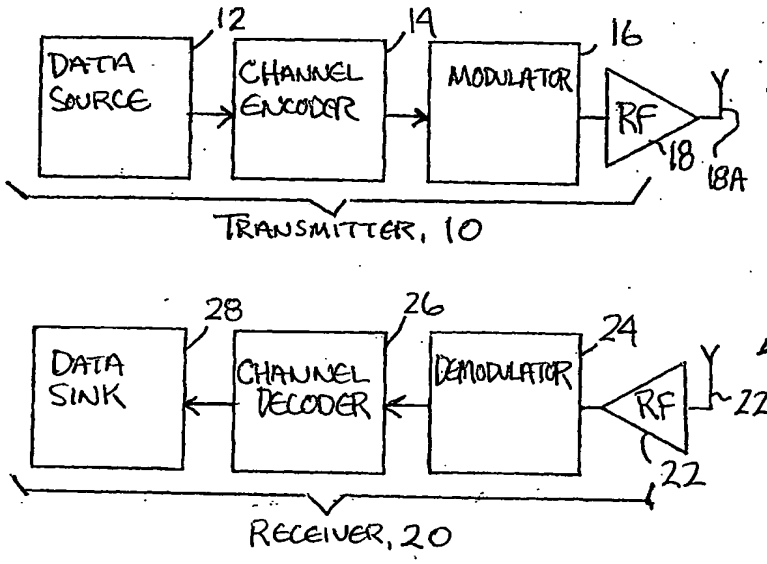

FIG. 1A
(PRIOR ART)

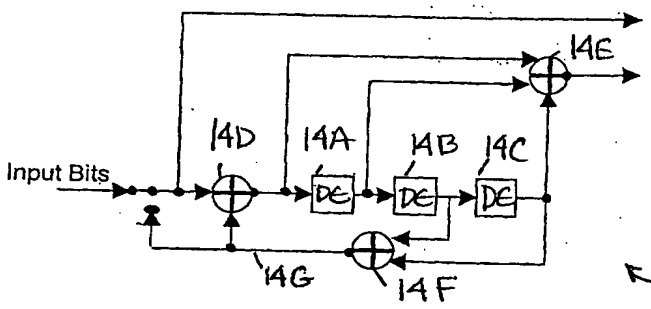

FIG. 1B
(PRIOR ART)

Input bit	Present encoder state	Next encoder state	State transition	Parity bit
0	000 (0)	000 (0)	0↔0	0
1	000 (0)	100 (4)	0↔4	1
0	001 (1)	100 (4)	1↔4	0
1	001 (1)	000 (0)	1↔0	1
0	010 (2)	101 (5)	2↔5	1
1	010 (2)	001 (1)	2↔1	0
0	011 (3)	001 (1)	3↔1	1
1	011 (3)	101 (5)	3↔5	0
0	100 (4)	010 (2)	4↔2	1
1	100 (4)	110 (6)	4↔6	0
0	101 (5)	110 (6)	5↔6	1
1	101 (5)	010 (2)	5↔2	0
0	110 (6)	111 (7)	6↔7	0
1	110 (6)	011 (3)	6↔3	1
0	111 (7)	011 (3)	7↔3	0
1	111 (7)	111 (7)	7↔7	1

FIG. 1C
(PRIOR ART)

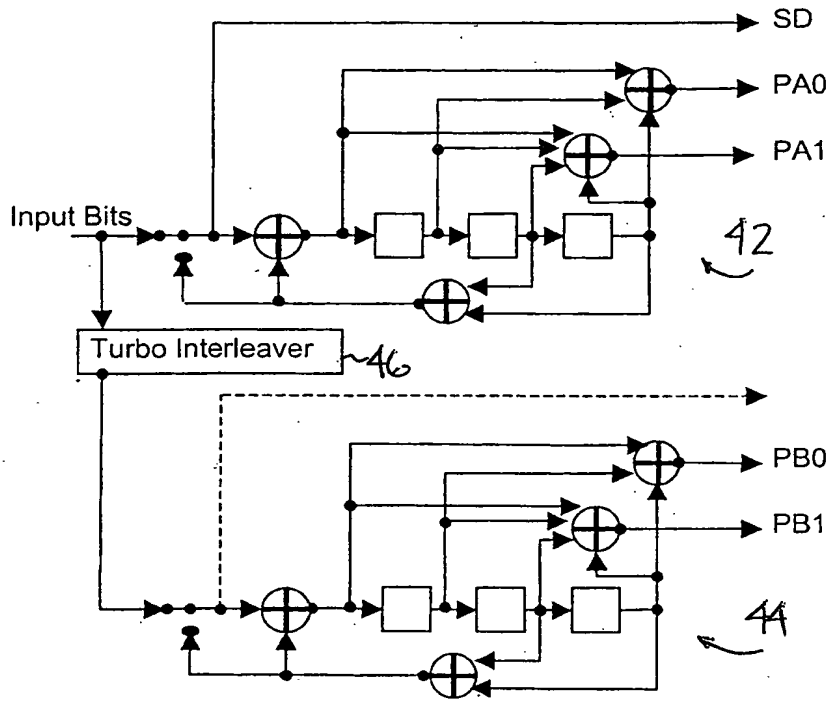

FIG. 2
40
(PRIOR ART)

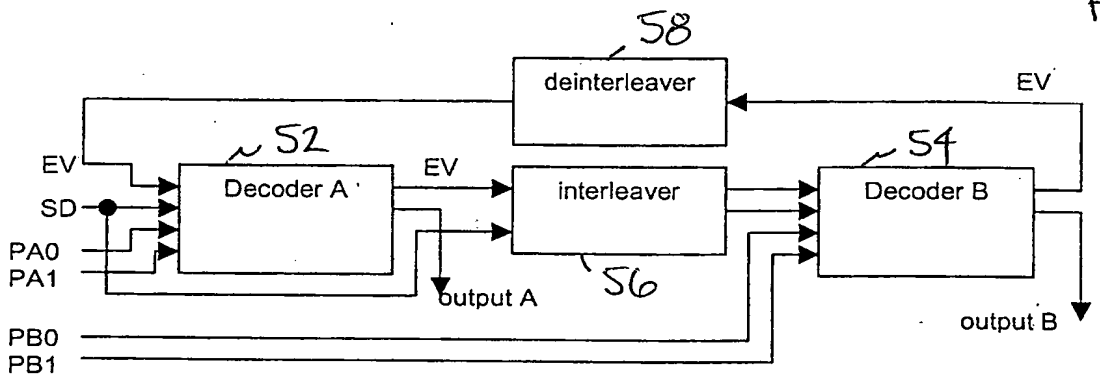

FIG. 3
50
(PRIOR ART)

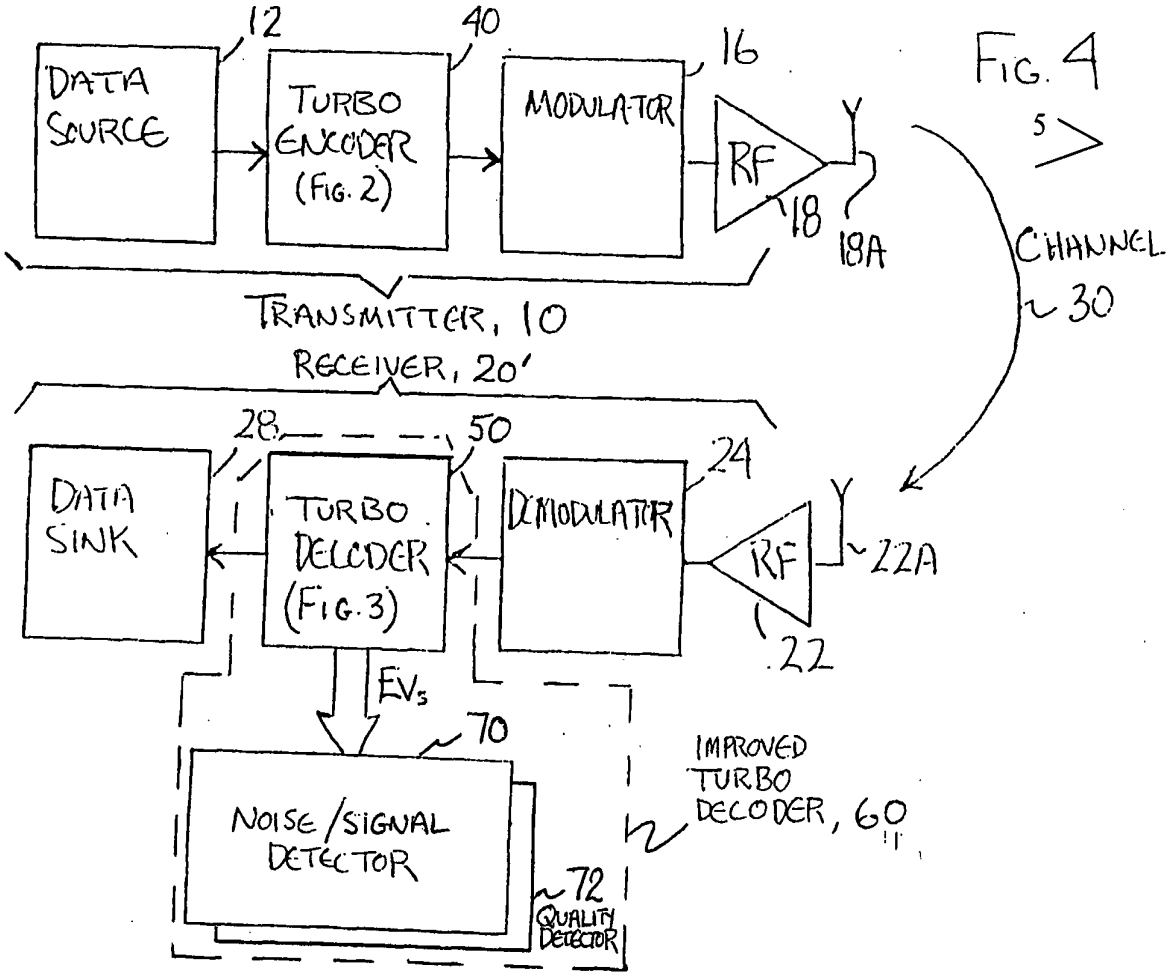
12
40
16
DATA SOURCE
TURBO ENCODER (FIG. 2)
MODULATOR
RF
Y
18
18A
TRANSMITTER, 10
CHANNEL
30
5
RECEIVER, 20'
28
50
24
DATA SINK
TURBO DECODER (FIG. 3)
DEMODULATOR
RF
Y
22A
22
EVs
70
IMPROVED TURBO DECODER, 60
NOISE/SIGNAL DETECTOR
72
QUALITY DETECTOR

FIG. 4